Objective

- Finding a phylogenetic tree that best explains the evolutionary relationship among a given set of species is computationally complex because of the greater than exponential search-space (real, multi-dimensional) and floating point arithmetic computation.

Why Network-on-Chip?

- Phylogenetic tree reconstruction is data/computation intensive.
- Use parallelism: Divide into a large number of smaller semi-independent sub-problems that can be computed concurrently.

NoC

Experimental Setup

- Computation core
  - Datapath: 64 bit
  - Number representation accuracy of 2-12 using Fixed-Point Hybrid Number System
  - All components designed with Verilog HDL and synthesized with 65 nm standard libraries
- Multi-core System
  - Interconnects laid out, parasitics (resistance, capacitance) extracted to determine physical parameters (power dissipation, delay)
  - N=16 and N=64 system sizes simulated using TreeSim
  - 32 lane PCIe 2.0 interface (5 Gbps)
- Software
  - RAxML-VI-HPC (version 7.0.4) on three inputs sourced from 2,177-taxon 68-gene mammalian dataset
  - Pentium IV 3.2 GHz dual-core CPU; GNU gprof utility for profiling
  - Best software runtime used as the baseline
  - Functions coreGTRCAT (f3) (48%), newviewGTRGAMMA (f3) (21%), and newviewGTRCAT (f5) (17%) collectively account for more than 85% of the total runtime

Multi-core System Design

Results

- Function-level speedup across different NoC architectures
- Variation of partition dispersion and function communication latency across different NoC architectures

Summary

- Network-on-Chip (NoC) based multi-core platform for accelerating Maximum Likelihood (ML) based phylogeny reconstruction
- Chief contributions
  - Design of a fine-grained parallel PE architecture
  - Novel algorithm to dynamically allocate nodes to tasks based on Hilbert space-filling curves
  - Design and extensive evaluation of different 2-D and 3-D NoC architectures
- Function-level speedup of ~847x, aggregate speedup of the accelerated portion up to ~6,500x, and overall run-time reduction of more than 5x over multithreaded software; exceeds the performance of all state-of-the-art hardware accelerators for this application class.